IC simulates matched transistor pairs

100 units on die are randomly paired for statistical matching; technique said to yield improved amplifiers, loggers, multipliers

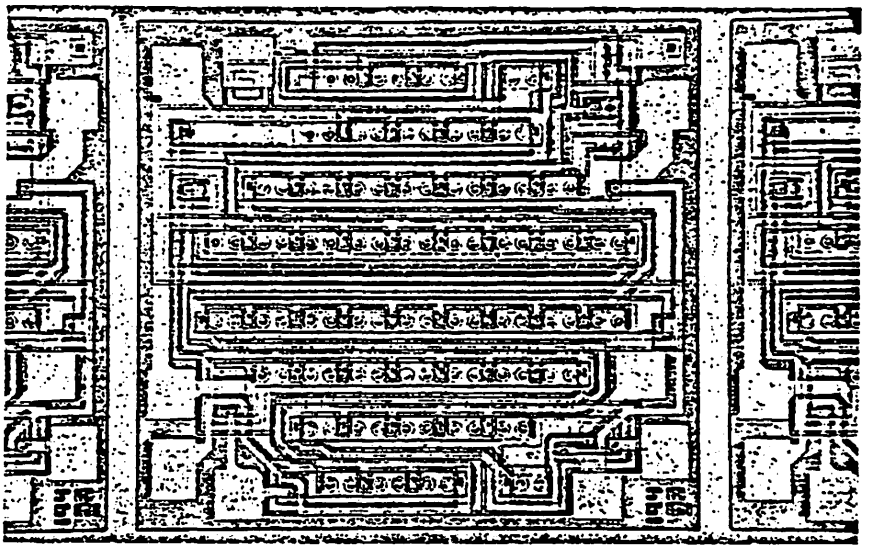
by Bernard Cole, San Francisco bureau manager

In a departure from traditional techniques, National Semiconductor Corp. has built what is essentially an integrated circuit that simulates the function of a matched transistor pair. The matching that results from the device—designated the LM194/394—is 10 to 60 times better than present transistor pairs, according to the company.

An unsung workhorse of the electronics industries, matched transistor pairs are used in many dc biasing jobs such as in instrumentation and power supplies, as well as in rf applications. They are usually made by fabricating two monolithic npn transistors on the same 600-to-800-square-mil die and trying to match their offsets. This approach has yielded transistor pairs matched within 0.5 to 3 millivolts.

What National has done with the LM194/394, says Carl Nelson, advanced-linear designer, is fabricate 100 npn monolithic transistors onto a die that is about 2,500 square mils in area and connect 25 pairs in parallel with the other 25. "But rather than attempting to match offsets," he says, "the attempt is made to randomly interconnect the 50 pairs of transistors to take advantage of statistical variations and random cancellation of offsets."

Even though any one pair may have offsets whose match varies between 0.5 and 3 millivolts, the net effect for all the 50 pairs is an offset matching to within 50 microvolts. "The matching gets closer to zero as the number of pairs in parallel goes up," he says. "More accurately, matching improves as a direct ratio of the square root of the number of transistors." A 100-transistor



matched-pair simulation, Nelson says, therefore offers a ten-fold improvement in performance over standard matched pairs on a die that is only two to four times larger.

Electrical characteristics of the LM194/394, such as drift versus initial offset voltage, noise, and the exponential relationship of the emitter-base voltage to the collector current, he says, "closely approach those of a theoretical transistor." On top of the 50-μV matching, offset voltage drift in dc amplifiers is held to 0.1 μV/°C (versus 2 μV for most transistor pairs). The IC circuit has a minimum current gain of 500, a current-gain match within 2%, and a common-mode rejection ratio of 120 to 130 decibels, compared with the 100 dB of conventional matched pairs.

Another product of the statistical matching of transistor pairs, he adds, "is a device with virtually only theoretical noise, enhancing its usefulness in ac amplifiers and nonlinear circuitry." Most of the parameters are guaranteed over a current range of 1 to 10 microamperes and a collector-base voltage from 0 to 40 V.

To guarantee long-term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation from reverse-biased emitter current, the most common cause of field failures in matched devices, Nelson says. "The parasitic isolation junction formed by the diodes also ensures isolation between devices," the designer adds.

Available in an isolated-header, six-lead TO-5 package, the LM194/394 is priced at $2.75 each for devices specified for operation from 0°C to 70°C.

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